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High Performance Vedic Multiplier Design using Compressors

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Abstract: This paper presents the design of high performance Vedic multiplier using compressors. The three major trepidations of designing digital circuits are area, speed and power. With advancing technology, encumbrance is being laid on attaining high speed, low power and less area. Multiplier is designed based on Vedic mathematics which has enhanced the performance of the circuit. In this paper, a new technique is introduced for 4:2 compressor and 5:2 compressor to mend the performance of the multiplier. The conventional circuits include designing with XOR modules which has improved performance over the full adders. In this paper, the compressor is designed using multiplexers which have shown advanced performance over the existing techniques. The design is implemented using Cadence EDA tools and area and timing have been calculated. The proposed technique has obtained 8.4 % reduction in area and 27.7 % improvement in PDP compared to the previous technique.

Keywords: Vedic, Compressor, Multiplexer

I. INTRODUCTION

Speed, power and area are the three major concerns of designing a digital circuit. Multipliers are most abundantly used components in Digital Signal Processor (DSP) and Arithmetic circuits. The speed of operation of the multiplier decides the speed of the processor. The existing multiplier techniques take various steps to attain the result because it is based on shift and add algorithm.

With progression in technology, speed is the major concern of design for which these techniques are not likely. Compressors are being used for multiplier design for improvement in speed [1]. Compressors can be designed in a number of techniques for attaining the required performance [2].

Multiplier is designed using Vedic mathematics technique for an improved performance [3, 8]. Basically compressors can be designed using full adders, XOR modules, etc. One of the other existing techniques is using a XOR-XNOR module which has further intensified the performance of the multiplier [4, 5].
Using this technique, there is a contribution of delay reduction, low power consumption and usage of less number of transistors [6]. To obtain high speed and low power, optimization has to be done at all abstraction levels [7].

The multiplier is designed based on the ancient Vedic mathematics which reduces the typical calculations in conventional techniques to simpler ones. Vedic mathematics is an approach of arithmetic rules for high speed implementation. The Vedic multiplier is implemented using Urthva Tiryakbhyam Sutra which means "Vertically and crosswise".

II. VEDIC MATHEMATICS

There are 16 different sutras of Vedic mathematics that can be applied to any branch of mathematics like algebra, trigonometry, etc.

The word 'Veda' is derived from Sanskrit which means 'knowledge'. Vedic mathematics is reconstructed by Sri Bharti Krishna Tirathaji based on his study on Vedic sutras between 1911 and 1918.
The Vedic mathematics is constructed on the operation of the human mind making the calculations simpler, which in turn reduces power consumption and area occupancy of the design.

Of the sixteen sutras, one sutra is considered for designing a multiplier, i.e., Urthva Tiryakbhyam sutra. 'Urthva' means 'Vertical' and 'Tiryak' means 'Crosswise'.

The illustration of a 4-bit multiplier can be shown here:

$$P_0=a_0b_0$$

$$P_1=a_0b_1+a_1b_0$$

$$P_2=a_2b_0+a_1b_1+a_0b_2$$

$$P_3=a_3b_0+a_2b_1+a_1b_2+a_0b_3$$

$$P_4=a_3b_1+a_2b_2+a_1b_3$$

$$P_5=a_3b_2+a_2b_3$$

$$P_6=a_3b_3$$

$$P_7=\text{carry at } P_6$$

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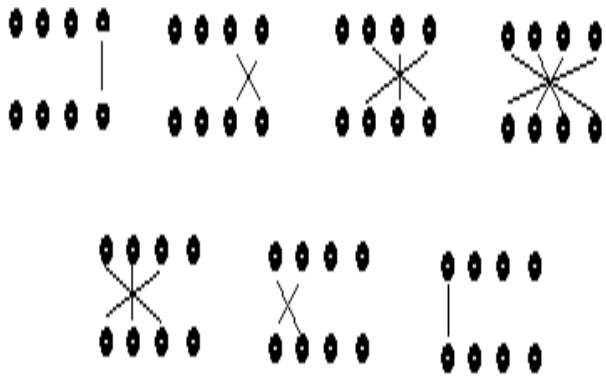

Fig. 1: Line diagram of a 4*4 multiplication

III. COMPRESSOR

An adder which can add more than 3 bits at a stretch i.e., which can add four to seven bits at a time is a compressor. The number of full adders and half adders are reduced so that the power consumption is reduced also improving the delay performance of the circuit. The compressors used in this paper are 4:2 compressor and 5:2 compressor.

a) 4:2 COMPRESSOR

The 4:2 compressor has 4 inputs (A, B, C and D) and 2 outputs (Sum & Carry) along with a Carry-in (Cin) and a Carry-out (Cout) as shown in Figure 2. The input Cin is the output of the neighboring lower significant compressor. The Cout is the input to the next significant stage compressor.

The 4:2 compressor operates based on the equation

$$\textbf{Sum= ((A} \oplus \textbf{B)} \oplus \textbf{(C} \oplus \textbf{D)} \oplus \textbf{Cin)}$$

$$\textbf{Carry= (}\overline{A \oplus B \oplus C \oplus D}\textbf{) D + (A} \oplus \textbf{B} \oplus \textbf{C} \oplus \textbf{D) Cin}$$

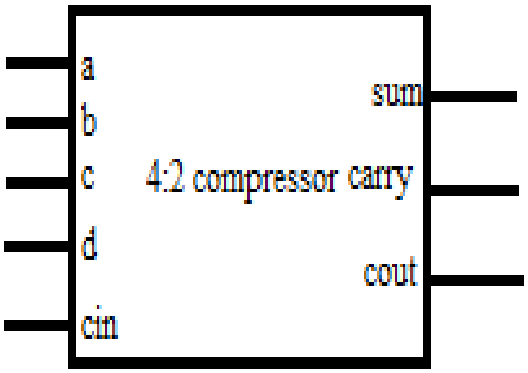

Fig. 2: Block Diagram of 4:2 Compressors

There are a number of ways to design a 4:2 compressor. The existing techniques represent 4:2 compressors using full adders and XOR modules. Using full adders, the critical path would be equal to 4 XOR gate delays. The critical path can be reduced to 3 XOR gate delays using XOR delays.

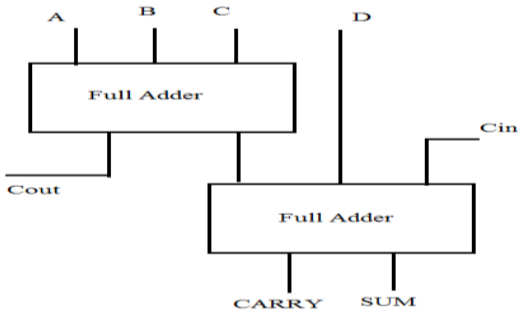

Fig. 3: 4:2 compressor using full adders

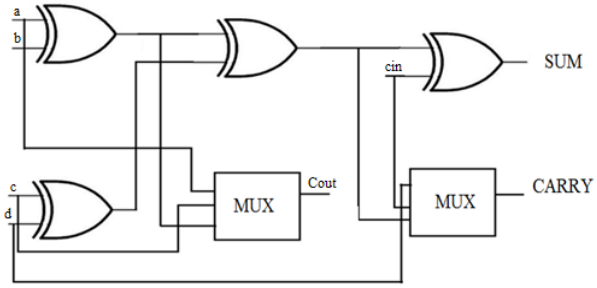

Fig. 4: 4:2 compressor using XOR modules

To further improve the performance, this paper presents the implementation of multiplier using MUX modules. Using this implementation, the performance is improved over the existing techniques.

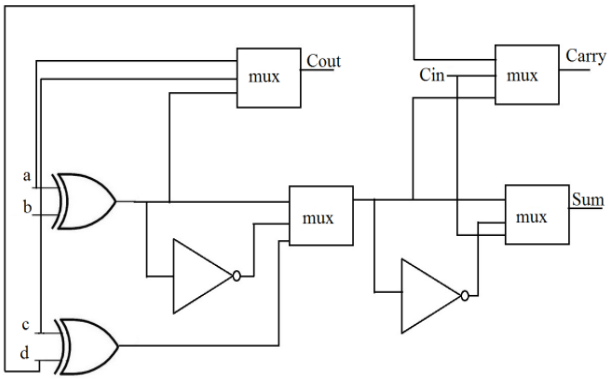

Fig. 5: Proposed 4:2 compressor circuit

b) 5:2 COMPRESSOR

The 5:2 compressor is another widely used building block for high precision and high speed multipliers. The basic block diagram of a 5:2 compressor is shown in Figure 6, which has seven inputs and four outputs. Five inputs are the primary inputs x1, x2, x3, x4 and x5, and the other two inputs Cin1and Cin2 receive their values from the neighboring compressor of one binary bit lower order in significance.

The 5:2 compressor operates based on equation

$$\textbf{Sum= (((((A} \oplus \textbf{B)} \oplus \textbf{(C} \oplus \textbf{D))} \oplus \textbf{E)} \oplus \textbf{Cin1)} \oplus \textbf{Cin2)}$$

$$\textbf{Carry= (}\overline{A \oplus B \oplus C \oplus D \oplus Cin1}\textbf{)E+(A} \oplus \textbf{B} \oplus \textbf{C} \oplus \textbf{D} \oplus \textbf{Cin1)Cin2}$$

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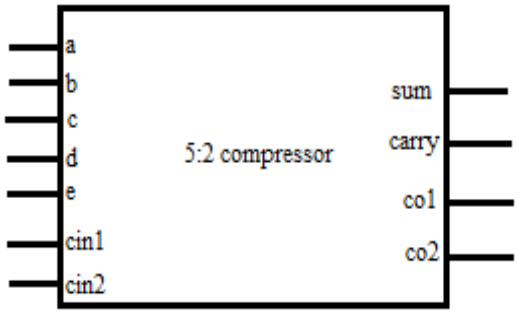

Fig. 6: Block Diagram of 5:2 compressor

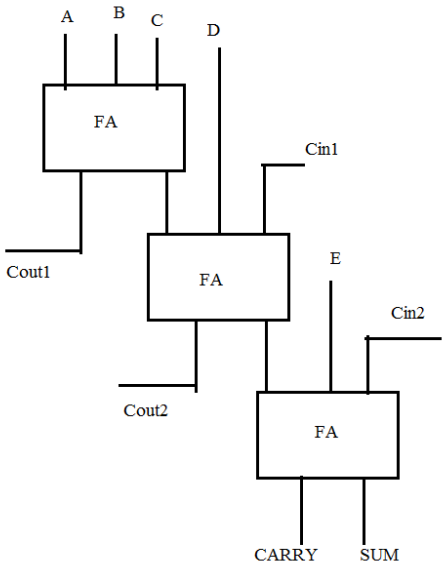

Fig. 7: 5:2 compressor using full adders

The representation of 5:2 compressor using full adders is shown in figure 7. The critical path is obtained as 6 XOR gate delays. This can be reduced to 5 XOR gate delays by designing the compressor using XOR modules. The design is shown in figure 8.

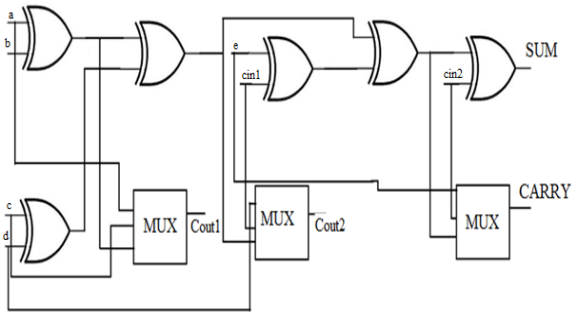

Fig. 8: 5:2 compressor using XOR modules

In the proposed architecture changes are to be made, to efficiently use the generated outputs at every stage. To obtain efficient output, few XOR blocks are replaced by XOR blocks with MUX blocks. In the proposed architecture these outputs are utilized efficiently by using multiplexers at select stages in the circuit.

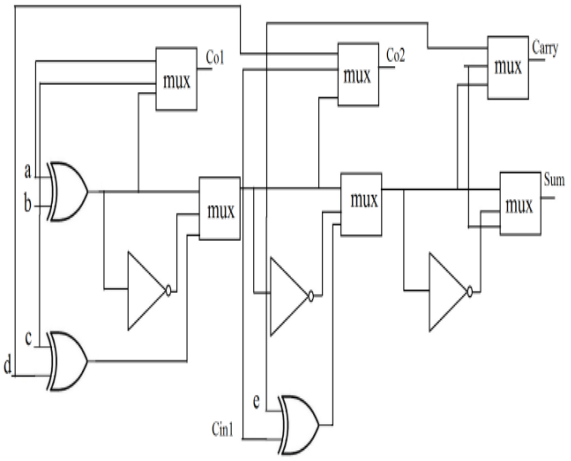

Fig. 9: Proposed 5:2 compressor circuit

IV. VEDIC MULTIPLIER USING COMPRESSORS

The multiplier implementation involves a number of full adders and half adders, so it produces a larger propagation delay. In our proposed model, we combined the Vedic multiplier with the proposed compressor technique. The block diagram of the implemented multiplier is shown in Figure 10.

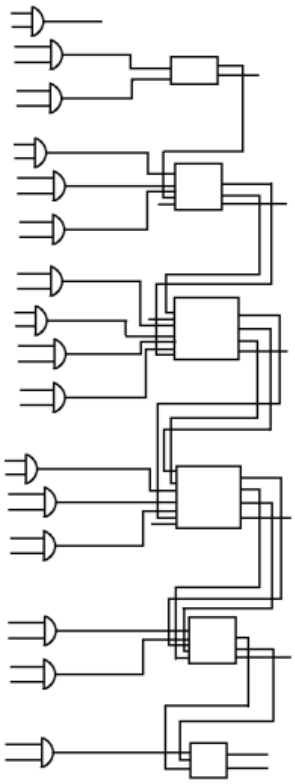

Fig. 10: Schematic of Vedic multiplier using Compressors

V. SIMULATION RESULTS

In this paper the results are simulated using Cadence RTL Compiler.

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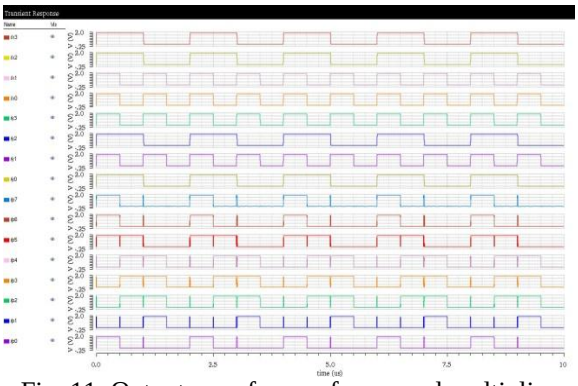

Fig. 11: Output waveforms of proposed multiplier

Table 1: Power and delay comparisons of various multiplier techniques

Multiplier Techniques	Power (µw)	Delay (ns)	PDP
Multiplier	5.43	2.525	13.71
Vedic Multiplier	0.172	3.132	5.38
Vedic Multiplier using Compressor (Technique 1)	1.58	2.669	4.21
Vedic Multiplier using Compressor (Technique 2)	0.502	2.381	1.19
Vedic Multiplier using Compressor (Proposed Technique)	0.36	2.398	0.86

The layout of the proposed multiplier is designed using a Cadence tool which is represented in figure 12.

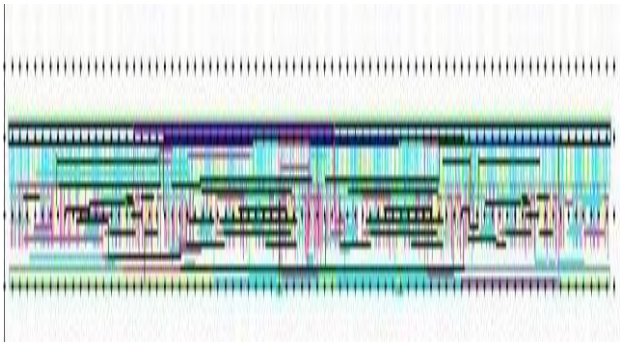

Fig. 12: Layout of Proposed multiplier

Table 2: Area Comparison of the multiplier techniques

Multiplier using Compressors	Area (in μm^2)
Vedic Multiplier using Compressor (Technique 1)	5181.11
Vedic Multiplier using Compressor (Technique 2)	4176.45
Vedic Multiplier using Compressor (Proposed Technique)	3823.89

VI. CONCLUSION

In order to achieve the requirements of Digital design, this paper presented the implementation of multiplier using Vedic mathematics. Compared to the regular array multiplier, the performance is quite improved using the Vedic mathematics. For further improvement in performance, compressors are used instead of full adders. As a result, the number of adders is reduced to a great extent. So the power and delay have shown better performance. There are three techniques discussed in this paper. The first technique is the implementation of compressors using full adders. The second technique is that compressors are implemented using XOR modules. The proposed circuit of compressors is using multiplexers which have reduced the number of logic gates. So this circuit has shown a better performance compared with the existing techniques.

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